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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/965,286	11/06/1997	TAKAYUKI GOMI	P97.2608	3718

26263 7590 04/24/2002

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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/965,286	GOMI ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6 and 20-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6 and 20-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The finality of the rejection of the last Office action is withdrawn in view of the new grounds of rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 3, 4, 6 and 20-26 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification recites on page 19 that the second embedded diffusion layer is diffused into a lower part of the epitaxial layer. The method of making the device recites that the second embedded diffusion layer is diffused as far as the interface between the epitaxial layer and the substrate (page 25). Figures 5 and 8 also depict the second embedded diffusion layer is diffused as far as the interface between the epitaxial layer and the substrate. Thus, there is no adequate description in the disclosure for a second embedded diffusion layer being diffused into a lower part of the epitaxial layer, as recited in claim 1, in such a way as to enable one

skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4. Claims 3, 22 and 27-29 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5. There is no support for a bottom of the first embedded diffusion layer being formed at a smaller distance from the datum surface than the midpoint of the second embedded diffusion layer, as recited in claim 3.

6. There is no support for a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the datum surface that is approximately equal to a location of the bottom of the first embedded diffusion layer from the datum surface, as recited in claim 22.

7. There is no support for a first speed height of the high speed base layer is equal to the first voltage height of the high voltage base layer, as recited in claim 27.

8. There is no support for a high voltage base layer comprising a lower surface that faces the second surface of the high voltage diffusion layer, wherein the first surface of the high voltage diffusion layer disposed at a second height, and wherein the second height is substantially at the datum, as recited in claim 27.

9. There is no support for a first surface of the high voltage diffusion layer disposed at a second height, wherein the second height is substantially at the datum, wherein the high voltage base layer comprising a lower surface that faces the second surface of the high voltage diffusion layer, as recited in claim 27.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 22 and 27-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. The claimed limitation of each impurity concentration of the high voltage diffusion layer being located between the high voltage peak impurity concentration (HVPIC) and the datum, as recited in claim 27, is unclear as to the location of the each impurity concentration of the high voltage diffusion layer, since the impurity concentration is located between a concentration (HVPIC) and a datum.

13. The claimed limitation of a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the datum surface that is approximately equal to a location of the bottom of the first embedded diffusion layer from the datum surface, as recited in claim 22, is unclear as how a distance between two elements can be approximately equal to a location of an element.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1, 3, 4 and 20-25, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Kumamaru et al. (4,379,726). Regarding claim 1, Kumamaru et al. teach in figure 10 a semiconductor device having a first vertical bipolar transistor 15 and a second vertical type transistor 13 having a breakdown voltage that is higher than that of the first vertical type transistor, formed on a P type semiconductor substrate comprising a first conductivity type silicon substrate 1, 5 defining a datum, an epitaxial layer 11 formed on the substrate above the datum surface, a first embedded diffusion layer 14 formed as part of a first vertical bipolar transistor 15 in a first upper part of the substrate and in the epitaxial layer and has the same conductivity type and higher impurity concentration than that of the epitaxial layer, a second embedded diffusion layer 13 (see figure 8) formed as part of a second vertical type transistor 13 directly on the substrate in a second upper part of the substrate and within a lower part of the epitaxial layer (column 3, lines 23-26), wherein the first embedded diffusion layer is not disposed within the second embedded diffusion layer, and having opposite conductivity type as that of the substrate and having an

impurity concentration less than the impurity concentration of the first embedded diffusion layer 14 and is approximately equal to or higher than the impurity concentration of the epitaxial layer (column 3, lines 16 and 27-28), and wherein peak positions of impurity concentrations of the first and second embedded diffusion layers reside at first and second distances from the datum surface of the substrate, such that the first distance is greater than the second distance.

Although figure 10 of Kumamaru et al. does not depict a second embedded diffusion layer 13 being formed within a lower part of the epitaxial layer 11, Kumamaru et al. teach in column 3, lines 23-26, that the second embedded diffusion layer 13 is formed within a lower part of the epitaxial layer 11.

Although Kumamaru et al. does not state that the peak positions of impurity concentrations of the first and second embedded diffusion layers reside at first and second distances from the datum surface of the substrate, respectively, such that the first distance is greater than the second distance, this feature is inherent in Kumamaru et al.'s device for the following reasons. The broad recitation of the claim does not require the datum surface to be located at the bottom surface of the substrate. The datum surface can be located at the top or the bottom surface of the substrate. Therefore, regardless the location of the peak positions of impurity concentrations of the first and second embedded diffusion layers, the datum surface can be considered at a location wherein the first distance is greater than the second distance. Thus,

Kumamaru et al. teach the peak positions of impurity concentrations of the first and second embedded diffusion layers reside at first and second distances from the datum surface of the substrate, respectively, such that the first distance is greater than the second distance, as claimed.

Regarding claim 3, Kumamaru et al. teach a bottom of the first embedded diffusion layer 14 being formed at a smaller distance from the datum surface (the interface between layers 11 and 5) than the midpoint of the second embedded diffusion layer. Note that the broad recitation of the claim does not require the datum surface to be the bottom surface of the substrate.

Regarding claims 4 and 21, although figure 10 of Kumamaru et al. does not depict a second embedded diffusion layer having impurity concentration portions that are equal and greater than that of the epitaxial layer, this feature is inherent in Kumamaru et al.'s device, because it is well known in the art that diffused areas have concentration that follows natural distribution curve, of which official notice is taken (See Watanabe et al.' figure 9, graph 22"). In the alternative, the second embedded diffusion layer can comprise layers 13 and 12. Thus, the second embedded diffusion layer has impurity concentration portions that are equal and greater than that of the epitaxial layer, as claimed.

Regarding claim 22, Kumamaru et al. teach a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the datum surface that is approximately equal to a location of the bottom of the first embedded diffusion layer from the datum surface, since the datum surface can be located at a position such that a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the datum surface that is approximately equal to a location of the bottom of the first embedded diffusion layer from the datum surface.

Regarding claim 23, Kumamaru et al. teach a first vertical type bipolar transistor defining a voltage that is different than that of the second vertical type bipolar transistor, wherein the first embedded diffusion layer having an impurity concentration that is higher than that of the epitaxial layer.

Regarding claims 20 and 24, Kumamaru et al. teach substantially the entire claimed structure, as applied to claim 1 above, including first and second bases disposed between two first and second graft base layers, above the first and second embedded diffusion layers to define first and second epitaxial thicknesses, respectively, wherein the first thickness is less than the second thickness, and wherein only the epitaxial layer is disposed between the base layer and the second embedded diffusion layer.

16. Claims 1, 3, 4, 21-23 and 25, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (4,258,379). Watanabe et al. teach in figure 8 a semiconductor device having a first vertical bipolar transistor 101 and a second vertical type transistor 201 having a breakdown voltage that is higher than that of the first vertical type transistor, comprising a first conductivity P type silicon substrate 1 defining a datum bottom surface, an epitaxial layer 3 formed on the substrate above the datum surface, a first embedded diffusion layer 21 formed as part of a first vertical bipolar transistor 101 in a first upper part of the substrate and in the epitaxial layer and has the same conductivity type and higher impurity concentration than that of the epitaxial layer, a second embedded diffusion layer 22" formed as part of a second vertical type transistor directly on the substrate in a second upper part of the substrate and within a lower part of the epitaxial layer, wherein the first embedded diffusion layer is not disposed within the second embedded diffusion layer, and having opposite conductivity type as that of the substrate and having an impurity concentration less than the impurity concentration of the first embedded diffusion layer and is approximately equal to or higher than the impurity concentration of the epitaxial layer (figure 9), wherein peak positions of impurity concentrations of the first and second embedded diffusion layers reside at first and second distances from the datum surface of the substrate, such that the first distance is greater than the second distance.

Although figure 8 of Watanabe et al. does not clearly depict a second embedded diffusion layer 22" being formed within a lower part of the epitaxial layer 3, figure 9 clearly shows a second embedded diffusion layer 22" being formed within a lower part of the epitaxial layer 3.

Regarding claim 3, Watanabe et al. teach in figure 9 a bottom of the first embedded diffusion layer 21 being formed at a smaller distance from the datum surface than the midpoint of the second embedded diffusion layer 22".

Regarding claims 4 and 21, Watanabe et al. teach in figure 9 a second embedded diffusion layer having impurity concentration portions that are equal and greater than that of the epitaxial layer.

Regarding claim 22, Watanabe et al. teach a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the datum surface that is approximately equal to a location of the bottom of the first embedded diffusion layer from the datum surface, since the datum surface can be located at a position such that a peak position of an impurity concentration of the second embedded diffusion layer resides at a distance from the datum surface that is approximately equal to a location of the bottom of the first embedded diffusion layer from the datum surface.

Regarding claim 23, Watanabe et al. teach a first vertical type bipolar transistor defining a voltage that is different than that of the second vertical type bipolar transistor, wherein the first embedded diffusion layer having an impurity concentration that is higher than that of the epitaxial layer.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 6, and 26, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (4,258,379). Regarding claim 6, Watanabe et al. teach substantially the entire claimed structure, as applied to claim 6 above, including a datum surface being the bottom surface of the substrate. Watanabe et al. do not teach a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15 in Watanabe et al.'s

device, since it is within the skills of an artisan to form a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15, subject to routine experimentation and optimization. Note that generally, differences in concentration or temperature do not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele , 406 F.2d 1403, 160 USPQ 809 (CCPA 1969). For more recent cases applying this principle, see Merck & Co. Inc . v. Biocraft Laboratories Inc. , 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied , 493 U.S. 975 (1989), and In re Kulling , 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990).

Regarding claim 26, it is conventional to reverse the polarity of the transistor. Therefore, it would be obvious to reverse the polarity, as claimed.

19. Claim 26, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al.

Kumamaru et al. teach substantially the entire claimed structure, as applied to claim 6 above, except reversing the polarity of the transistor. It would have been obvious to a

person of ordinary skill in the art at the time the invention was made to reverse the polarity of the transistor, because it is conventional to reverse the polarity of the transistor of which official notice is taken.

20. Claims 6 and 27-29, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al. in view of Watanabe et al.

Regarding claim 27, Kumamaru et al. teach in figure 8 a semiconductor device comprising a substrate 1 having a first surface that defines a datum, a high speed diffusion layer 14 comprising a first surface disposed above the datum at a first height, a high voltage diffusion layer 13 (see figure 8) comprising a first surface disposed at a second height, wherein the second height is substantially at the datum, a high speed base layer 21 comprising a lower surface that faces the first surface of the high speed diffusion layer and is disposed at a first speed height from the datum; a high voltage base layer 17 comprising a lower surface that faces the second surface of the high voltage diffusion layer and is disposed at a first voltage height from the datum, wherein the first speed height of the high speed base layer is equal to the first voltage height of the high voltage base layer; an epitaxial layer 11, wherein the epitaxial layer is disposed between the first surface of the high speed diffusion layer and the lower surface of the high speed base layer, and wherein only the epitaxial layer is disposed

between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer, wherein the high speed (HS) diffusion layer comprises a peak impurity concentration (HSPIC) value and wherein the high voltage (HV) diffusion layer comprises a peak impurity concentration (HVPIC) value, such that the high voltage peak impurity concentration (HVPIC) value is less than the high speed peak impurity concentration (HSPIC) value, and wherein each impurity concentration of the high voltage diffusion layer that is located between the high voltage peak impurity concentration (HVPIC) and the datum can be higher than leach impurity concentration of the epitaxial layer that is located between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer.

Kumamaru et al. do not state the precise impurity concentration of the high voltage diffusion layer.

Watanabe et al. teach in figures 4 and 9 each impurity concentration of the high voltage diffusion layer that is located between the high voltage peak impurity concentration (HVPIC) and the datum is higher than leach impurity concentration of the epitaxial layer that is located between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to adjust the impurity concentration of the high voltage diffusion layer that is located between the high voltage peak impurity concentration (HVPIC) and

the datum to be higher than leach impurity concentration of the epitaxial layer that is located between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer in Kumamaru et al.'s device, in order to optimize working characteristics of the device. Note that generally, differences in concentration or temperature do not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele , 406 F.2d 1403, 160 USPQ 809 (CCPA 1969). For more recent cases applying this principle, see Merck & Co. Inc . v. Biocraft Laboratories Inc. , 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied , 493 U.S. 975 (1989), and In re Kulling , 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990).

Regarding claim 28, Kumamaru et al. and Watanabe et al. teach a high speed (HS) diffusion layer comprises a peak impurity concentration (HSPIC) value that is disposed at distance Yhspic below the datum, wherein the high voltage (HV) diffusion layer comprises a peak impurity concentration (HVPIC) value that is disposed at distance Yhvpic below the datum, wherein Yhvpic > Yhspic

Regarding claim 29, Kumamaru et al. teach in figure 8 an epitaxial layer between the first surface of the high speed diffusion layer and the lower surface of the high speed base layer defines a thin collector layer, wherein the epitaxial layer between the first surface of the high voltage diffusion layer and the lower surface of the high voltage base layer defines a thick collector layer, wherein the thick collector layer is thicker than the thin collector layer.

Regarding claim 6, Kumamaru et al. do not state that the datum surface being the bottom surface of the substrate, and a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15. Watanabe et al. teach that the datum surface being the bottom surface of the substrate, such that the peak positions of impurity concentrations of the first and second embedded diffusion layers reside at first and second distances from the datum surface of the substrate, so that the first distance is greater than the second distance. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a datum surface being the bottom surface of the substrate, such that the peak positions of impurity concentrations of the first and second embedded diffusion layers reside at first and second distances from the datum surface of the substrate, so that the first distance is greater than the second distance, and a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15 in Kumamaru et al.'s device, in order improve

the device performance and characteristics, and since it is within the skills of an artisan to form a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15, subject to routine experimentation and optimization, respectively. Note that generally, differences in concentration or temperature do not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele , 406 F.2d 1403, 160 USPQ 809 (CCPA 1969). For more recent cases applying this principle, see Merck & Co. Inc . v. Biocraft Laboratories Inc. , 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied , 493 U.S. 975 (1989), and In re Kulling , 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990).

Response to Arguments

21. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Ori Nadav

April 19, 2002